

### **REMARKS**

Claims 1-20 are pending. Claims 1 and 11 were amended to more particularly point out and distinctly claim the present invention. Withdrawal of the outstanding rejections is respectfully requested for at least the reasons set forth below.

#### ***Amendment to the Specification***

The specification was amended to correct obvious typographical errors and, therefore no new subject matter was added.

#### ***Rejection under 35 U.S.C. § 102(e)***

Claims 1, 7 and 11 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,954,463 (Ma et al.), hereinafter, "Ma."

Claims 1-2, 6-7 and 11-13 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,741,594 (Tzeng et al.), hereinafter, "Tzeng." The Applicants respectfully traverse the rejection for the reason listed below.

#### **1. Patentability of claims 1, 7 and 11 over Ma**

A. Amended independent claim 1 recites at least the following features that are not disclosed or suggested in Ma:

tracking a connection state of the switch with reference to the format of each of the frames, and  
storing the connection state in a memory register.

The present invention discloses tracking a connection state of the switch with reference to the format of each of the frames, wherein each of the frames are identified while being concurrently routed through a switch. Accordingly, the switch operation is controlled with reference to the identified format of each of the frames. During the operation of the switch, a connection state is tracked and is stored in a register memory of the switch. The connection state is referenced to the identified format of each of the frames as they are routed through the switch.

Fig. 6 and page 10, lines 12-16 of the present specification discloses a control section 603 of switch 600 that keeps track of the status of a connection state and stores it in a memory register, wherein the connection state is either "latch" or "lock" according to the format of each of the frames. The tracking and storing of the connection state of the switch is a dynamic process, which changes according to the identified format of each of the frames as they are routed through the switch.

In contrast, Ma does not disclose or suggest tracking a connection state of the switch with reference to the format of each of the frames and that a connection state is stored in a register memory.

B. Independent claim 7 recites at least the following feature that is not disclosed or suggested in Ma:

defining a dual-format frame for concurrently routing a plurality of frames through the switch

The present invention discloses the operating of a switch configured with connection states and defines a dual-format frame for concurrently routing a plurality of frames through the switch. Referring to Fig. 8 and page 13, lines 5-16 of the present specification discloses a dual-format frame 300-2 that comprises a frame header 801-2 for a large packet and a frame header 805 for a small packet. Specifically, Fig. 8 illustrates a dual-format frame that comprises a large packet header 801-2 that is the in-band control signal at one stage of the switching and which is consumed at that stage. In addition, frame 300-2 further comprises the payload of the large packet. The payload comprises a plurality of small packets (303-1, 303-2, 303-4, etc...) that comprises a small packet header 805 and a payload, thereby forming a dual-format frame.

In contrast, Ma does not disclose or suggest a dual-format frame for concurrently routing a plurality of frames through a switch. Column 5, lines 38-63 Ma discloses a variety of frame formats (e.g., VoIP, L2TP and PPP) and the processing, reformatting or modifying of the headers in the frames. However, none of these frames are dual-format frames.

C. Amended independent claim 11 recites at least the following feature that is not disclosed or suggested in Ma:

a means for tracking a connection state with reference to the format of each of the frames.

The present invention discloses a switch for concurrently routing frames, wherein the switch comprises a means for tracking a connection state with reference to the format of each of the frames. Referring to Fig. 6 and page 10, lines 14-19 of the current specification, the present invention discloses a control section 603 of the switch 600 that keeps track of a status of a connection state with reference to the format of each of the frames. Memory register 609 stores the status of the connection state, which may change accordingly as a result of the format of each of the frames that are routed through the switch.

In contrast, Ma does not disclose or suggest a means for tracking a connection state with reference to the format of each of the frames.

Therefore, in view of the difference between the present invention and that of Ma, amended independent claims 1 and 11, and claim 7 are believed to be patentable over Ma. Accordingly, the rejection of claims 1, 7 and 11 should be withdrawn.

## 2. Patentability of claims 1, 7 and 11 over Tseng

A. Amended independent claim 1 recites at least the following features that are not disclosed or suggested in Ma:

tracking a connection state of the switch with reference to the format of each of the frames, and  
storing the connection state in a memory register.

As previously described above, the present invention discloses tracking and storing a connection state of the switch with reference to the format of each of the frames. However, Tseng does not disclose or suggest tracking a connection state of the switch with reference to the format of each of the frames and storing the connection state in a memory register. Tseng discloses in column 5, lines 3-11 that each multiport switch 12 includes a switch fabric 25 that is

configured for making frame forwarding decisions for receiving data packets. Specifically, the switch fabric 25 is configured for layer 2 and layer 3 switching based on an IP data packet. However, Tzeng does not disclose or suggest that either multiport switch 12 or switch fabric 25 is used for tracking a connection state of the switch with reference to the format of each of the frames and then storing the connection state in a memory register.

Therefore, Tzeng does not suggest or disclose tracking a connection state of the switch with reference to the format of each of the frames, and storing the connection state in a memory register.

B. Independent claim 7 recites at least the following feature that is not disclosed or suggested in Ma:

defining a dual-format frame for concurrently routing a plurality of frames through the switch

As previously described above, the present invention discloses a dual-format frame. However, Tzeng does not disclose or suggest defining a dual-format frame for concurrently routing a plurality of frames through the switch. Column 4, lines 44-46 of Tzeng discloses data protocol formats IPv4 and IPv6 and column 5, lines 64-63 of Tzeng discloses HTTP and SNMP format data packets. However, none of these formats are defined as having a dual-format frame for concurrently routing a plurality of frames through the switch.

C. Amended independent claim 11 recites at least the following feature that is not disclosed or suggested in Tzeng:

...the switch comprising:

...  
a control circuit for controlling the operation of the switch with reference to the format of each of the frames, and  
...

The present invention discloses a control circuit for controlling the operation of the switch with reference to the format of each of the frames. Fig. 6 and page 10, line 21 to page 11,

line 14 of the present specification discloses a control section 603 that comprises a clock counter 602, a connection state circuitry 105 and a latch/lock status 609. A frame clock signal is inputted into the control section 603, which is also inputted into the clock counter 602, where the frame clock signal unlatches the connection state and triggers a frame-level control for the control section 603. A frame header at the beginning of the frame identifies the packet format to be either a large packet or a number of small packets. Aided by two memory registers, the clock counter 602, the latch/lock status 609 and the connection state circuitry 105 may or may not set the connection state during a frame-level control operation of the switch.

The Examiner states that element 74 in Fig. 4 and column 8, lines 16-30 of Tzeng disclose a switch comprising a control circuit for controlling the operation of the switch with reference to the format of each of the frames. Applicant respectively disagrees with this statement. Element 74 is a min term controller that is configured for fetching the min terms from the min term memory 70, in which the min terms correspond to a selected byte of the IP frame 32. Therefore, the min term controller is not a control circuit for controlling the operation of a switch. Fig. 4 is a block diagram illustrating details of a packet classifier 24, in which min term controller 74 is a part of the packet classifier 24, which, in turn, is a part of a switch port 20. Switch port 20 is not a switch, but a part (i.e., port) of the switch 12a. Therefore, min term controller 74 is a control circuit that is only used to fetch data (i.e., min terms) from memory for the packet classifier. Tzeng discloses in column 5, lines 14-16 that host CPU 26 controls the overall operations of switch 12, which includes programming the switch fabric 25. Referring again to Fig. 1, Tzeng discloses that the host CPU 26 is a separate element, which is externally connected to the switch 12, and thus the switch 12 does not comprise a control circuit for controlling the operation of the switch with reference to the format of each of the frames.

Therefore, in view of the difference between the present invention and that of Tzeng, amended independent claims 1 and 11, and claim 7 are believed to be patentable over Tzeng. Accordingly, the rejection of claims 1, 7 and 11 should be withdrawn.

3. Patentability of rejected dependent claims

The rejected dependent claims are believed to be patentable because they depend from allowable independent claims and because they recite additional patentable features. Accordingly, the rejection of dependent claims 2, 6, 12 and 13 should be withdrawn.

4. Allowable claims

Applicant notes that claims 10 and 17-20 are allowable, and that claims 3-5, 8-9 and 14-16 would be allowable if rewritten in independent form. Claims 3-5, 8-9 and 14-16 are still believed to be patentable over the applied references even though they were not amended to be in independent form, because they are dependent upon allowable independent claims, and because they recite additional patentable features.

*Conclusion*

Insofar as the Examiner's rejections were fully addressed, the instant application including claims 1-9 and 11-16 is in condition for allowance. A Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

Shuo-Yen Robert Li

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(Date)

CLARK A. JABLON  
Registration No. 35,039  
AKIN GUMP STRAUSS HAUER & FELD LLP  
One Commerce Square  
2005 Market Street - Suite 2200  
Philadelphia, PA 19103  
Direct Dial: (215) 965-1293  
Facsimile: (215) 965-1210

CAJ/PAI/gem

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